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1 An efficient ILP-based scheduling algorithm for control-dominated VHDL descriptions

Michael Münch, Norbert Wehn, Manfred Glesner

October 1997 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 2 Issue 4

Full text available: pdf(375.99 KB) Additional Information: full citation, abstract, references, index terms

To adopt behavioral synthesis techniques in existing design flows, the synthesis methodology must provide the designer with a mechanism to specify a component's interface timing. This will permit pre- and postsynthesis validation through cosimulation with other subsystems or even through formal verification. In control-flow dominated designs, additional timing constraints will result in a complex specification/constraint system for which the scheduling problem has been shown to be NP-comple ...

Keywords: integer linear programming (ILP), scheduling, timing constraints

2 Safety checking of machine code

Zhichen Xu, Barton P. Miller, Thomas Reps

May 2000 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2000 conference on Programming language design and implementation**, Volume 35 Issue 5

Full text available: pdf(306.71 KB) Additional Information: full citation, abstract, references, citings, index terms

We show how to determine statically whether it is safe for untrusted machine code to be loaded into a trusted host system. Our safety-checking technique operates directly on the untrusted machine-code program, requiring only that the initial inputs to the untrusted program be annotated with typestate information and linear constraints. This approach opens up the possibility of being able to certify code produced by any compiler from any source language, which gives the code prod ...

3 The priority-based coloring approach to register allocation

Fred C. Chow, John L. Hennessy

October 1990 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 12 Issue 4

Full text available: pdf(2.97 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Global register allocation plays a major role in determining the efficacy of an optimizing compiler. Graph coloring has been used as the central paradigm for register allocation in

modern compilers. A straightforward coloring approach can suffer from several shortcomings. These shortcomings are addressed in this paper by coloring the graph using a priority ordering. A natural method for dealing with the spilling emerges from this approach. The detailed algorithms for a priority-based colori ...

4 An Efficient ILP-Based Scheduling Algorithm for Control-Dominated VHDL Descriptions

Authors: Michael Muench, Manfred Glesner, Norbert Wehn

November 1996 **Proceedings of the 9th International Symposium on System Synthesis**

Full text available: pdf(940.81 KB) Publisher Site

Additional Information: full citation, abstract

In this paper, we present for the first time a mathematical framework for solving a special instance of the scheduling problem in control-flow dominated behavioral VHDL descriptions given that the timing of I/O signals has been completely or partially specified. It is based on a code-transformational approach which fully preserves the VHDL semantics. The scheduling problem is mapped onto an integer linear program (ILP) which can be constrained to be solvable in polynomial time, but still permits ...

Keywords: scheduling, control-flow dominated VHDL, ILP, time-constrainted scheduling, resource-constrained scheduling, code transformation

5 Phase coupling and constant generation in an optimizing microcode compiler

Steven R. Vegdahl

October 1982 **Proceedings of the 15th annual workshop on Microprogramming**

Full text available: pdf(831.84 KB) Additional Information: full citation, abstract, references, citings, index terms

The designer of an optimizing compiler must concern himself with the order in which optimization phases are performed; a pair of phases may be interdependent in the sense that each phase could benefit from information produced by the other. In a compiler for a horizontal target architecture, one such phase-ordering problem occurs between code-generation and compaction. Presented here is an overview of a research effort at Carnegie-Mellon University which ha ...

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1 **Partial redundancy elimination driven by a cost-benefit analysis**
Horspool, R.N.; Ho, H.C.;
Computer Systems and Software Engineering, 1997., Proceedings of the Eighth Israeli Conference on , 18-19 June 1997
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[Abstract] [PDF Full-Text (568 KB)] **IEEE CNF**

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2 **Resource-sensitive profile-directed data flow analysis for code optimization**
Rajiv Gupta; Berson, D.A.; Fang, J.Z.;
Microarchitecture, 1997. Proceedings. Thirtieth Annual IEEE/ACM International Symposium on , 1-3 Dec. 1997
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[Abstract] [PDF Full-Text (1012 KB)] **IEEE CNF**

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3 **A constructive method for exploiting code motion**
dos Santos, L.C.V.; Heijligers, M.J.M.; van Eijk, C.A.J.; van Eijndhoven, J.T.J.; Jess, J.A.G.;
System Synthesis, 1996. Proceedings., 9th International Symposium on , 6-8 Nov. 1996
Pages:51 - 56

[Abstract] [PDF Full-Text (652 KB)] **IEEE CNF**

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4 **Code optimization as a side effect of instruction scheduling**
Gupta, R.;
High Performance Computing, 1997. Proceedings. Fourth International Conference on , 18-21 Dec. 1997

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5 **Scheduling of conditional branches using SSA form for superscalar/VLIW processors**
Seong-Uk Choi; Sung-Soon Park; Myong-Soon Park;
Parallel and Distributed Systems, 1996. Proceedings., 1996 International Conference on , 3-6 June 1996
Pages:344 - 351

[Abstract] [PDF Full-Text (720 KB)] **IEEE CNF**

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6 **FACT: a framework for applying throughput and power optimizing transformations to control-flow-intensive behavioral descriptions**
Lakshminarayana, G.; Jha, N.K.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 , Issue: 11 , Nov. 1999
Pages:1577 - 1594

[Abstract] [PDF Full-Text (596 KB)] **IEEE JNL**

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7 **Compiling real-time programs with timing constraint refinement and structural code motion**
Gerber, R.; Seongsoo Hong;
Software Engineering, IEEE Transactions on , Volume: 21 , Issue: 5 , May 1995
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8 **Task response time optimization using cost-based operation motion**
Tabbara, B.; Tabbara, A.; Sangiovanni-Vincentelli, A.;
Hardware/Software Codesign, 2000. CODES 2000. Proceedings of the Eighth International Workshop on , 3-5 May 2000
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[Abstract] [PDF Full-Text (408 KB)] **IEEE CNF**

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9 **SPARK: a high-level synthesis framework for applying parallelizing compiler transformations**
Gupta, S.; Dutt, N.; Gupta, R.; Nicolau, A.;
VLSI Design, 2003. Proceedings. 16th International Conference on , 4-8 Jan. 2003
Pages:461 - 466

[Abstract] [PDF Full-Text (294 KB)] **IEEE CNF**

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10 **FACT: a framework for the application of throughput and power optimizing transformations to control-flow intensive behavioral descriptions**
Lakshminarayana, G.; Jha, N.K.;
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[Abstract] [PDF Full-Text (724 KB)] IEEE CNF

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11 **Efficient edge profiling for ILP-processors**
Eichenberger, A.E.; Lobo, S.M.;
Parallel Architectures and Compilation Techniques, 1998. Proceedings. 1998 International Conference on , 12-18 Oct. 1998
Pages:294 - 303

[Abstract] [PDF Full-Text (96 KB)] IEEE CNF

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12 **Concurrent SSA form in the presence of mutual exclusion**
Novillo, D.; Unrau, R.; Schaeffer, J.;
Parallel Processing, 1998. Proceedings. 1998 International Conference on , 10-14 Aug. 1998
Pages:356 - 364

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13 **Proceedings of the 1998 International Conference on Computer Languages (Cat. No.98CB36225)**

Computer Languages, 1998. Proceedings. 1998 International Conference on , 14-16 May 1998
[Abstract] [PDF Full-Text (828 KB)] IEEE CNF

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Hank, R.E.; Hwu, W.W.; Rau, B.R.;
Microarchitecture, 1995. Proceedings of the 28th Annual International Symposium on , 29 Nov.-1 Dec. 1995
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Landry, K.; Arthur, J.D.;
Computer Languages, 1994., Proceedings of the 1994 International Conference on , 16-19 May 1994
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www.ljosa.com/~ljosa/doc/encycmuclopedia/impl/compiler-implementation.txt - 266k - Cached

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www.few.vu.nl/~dick/Summaries/CS/CompilerConstruction1980-1989.html - 182k - Cached

7. http://www.city.palo-alto.ca.us/clerk/minutes/1997/19970922.html
... could move **forward** on the ... Municipal **Code" MOTION** PASSED 9 ... **first** paragraph under "Design Charact promote a design variety within the **breadth** ...
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11. http://www.iste.uni-stuttgart.de/ps/AdaBasis/pal_1195/ada/ajpo/testing/aces/html/zd_readg.txt
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14. Kirjastojärjestelmän raportti: Teokset ilman luokkaa
... 31.12.1975. hmt1773102. **First** version of a data flow procedure ... 12.1976. hmt1774373. On **forward** and bac hmt1773905. **Code motion**. 31.12.1980 ...
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